NEWSLETTER

INTERNATIONAL TUNGSTEN INDUSTRY ASSOCIATION

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Annual General Meeting 2004

The 17th Annual General Meeting of ITIA will be held in the Marriott Hotel, Lisbon during the week beginning 27 September 2004 with a provisional programme as follows:

Monday 27 September
Meetings of the HSEC and Executive Committee
Evening function

Tuesday 28 September
AGM half-day
Evening function

Wednesday 29 September
AGM half-day
Free evening

Thursday 30 September
Possible visit to the Beralt mine

Further information will be made available at the end of next April.

16th Annual General Meeting

It is 3 months since the 16th Annual General Meeting was held in Prague, generously hosted by Osram Bruntal / Sylvania Tungsten and Seco Tools / Pramet Tools and attended by 170 delegates from all over the tungsten world. It will therefore be sufficient to mention only that Bob Fillnow (Vice President Marketing at Osram Sylvania Products Inc.) was elected to succeed Dave Landsperger (Kennametal) as President and Zhu Guang (Senior Vice-President, China National Metals & Minerals Imp. & Exp. Corp.) was elected as Vice-President.

TECHNICAL SERVICE

In the June Issue, reference was made to the imminent introduction of this service, using a Consultancy comprising two Professors of the University of Vienna, Erik Lassner and Wolf-Dieter Schubert. It is now functioning with primary aims

- To improve the level of expertise available from ITIA to members and non-members.
- To increase the flow of technical information which might help to promote tungsten usage.
- To update the technical content of the ITIA's website.
- To expand the website in terms of the key properties of tungsten.
- To answer technical enquiries received by the Secretariat.
- To collect the latest information about new uses.
- To evaluate articles for inclusion on the website and in the Newsletter.
- To write technical articles for each edition of the twice-yearly Newsletter.
- To expand the members' directory into a matrix of companies and their main products to provide a more easily accessible database to which customers might direct their enquiries.

Readers are invited to submit to the ITIA Secretariat any papers or news items concerning new applications for tungsten. If the language is other than English, an abstract in English must be supplied with the original article.

TUNGSTEN IN INTEGRATED CIRCUITS

The Technical Consultancy makes its first contribution with the article below, taking the view that there are not so many people who know that tungsten is among the very important components in modern integrated circuitry.

Chips are not very old. Their development started around 1960 and went on avalanche-like as demonstrated in ***Table 1.*** As the number of electronic structures on a chip increased with time the structures became smaller and the circuit functionality increased enormously.

A chip or integrated circuit is a fingernail-sized piece of extremely pure silicon wafer-like layered with circuitry. These chips created the information age with all the electronic marvels which changed our world so dramatically. Storage and processing of information in a chip takes place in tiny electronic structures, mostly transistors. They act as electronic switches, which are interconnected to a high degree of complexity, enabling today almost any kind of computation. The demand for semiconductors and related equipment is still steadily growing. Main drivers of this demand for advanced chips are communications, consumer applications and computing. In 1999 the worldwide market for chips was worth approximately 150 billion US $ and by 2003 it is expected to double to over 300 billion US $.

Table 1: Maximum number of transistors in an Integrated Circuit and driving forces for chip development

1960s	10^3	
1970s	$10^3 – 5.10^4$	watches and pocket calculators
1980s	5.10^4 - 10^6	PC
1990s	$10^6 – 5.10^7$	PC, network, internet, telecommunication
2000+	≥ 5.10^7	mobile telecom, internet
2010 Forecast	10^9-10^{10}	

A chip has a complicated, multilayered structure which consists of different metals, semiconductors and dielectrics in different shapes ***(see Fig. 1)***. Chip production is a very complex manufacturing process involving hundreds of steps and all of them have to be performed under extreme precision and cleanliness. Operations are performed by computer controlled robotic devices in "clean rooms" that are a thousand times cleaner than a hospital operating room. All raw materials have to be of special purity.

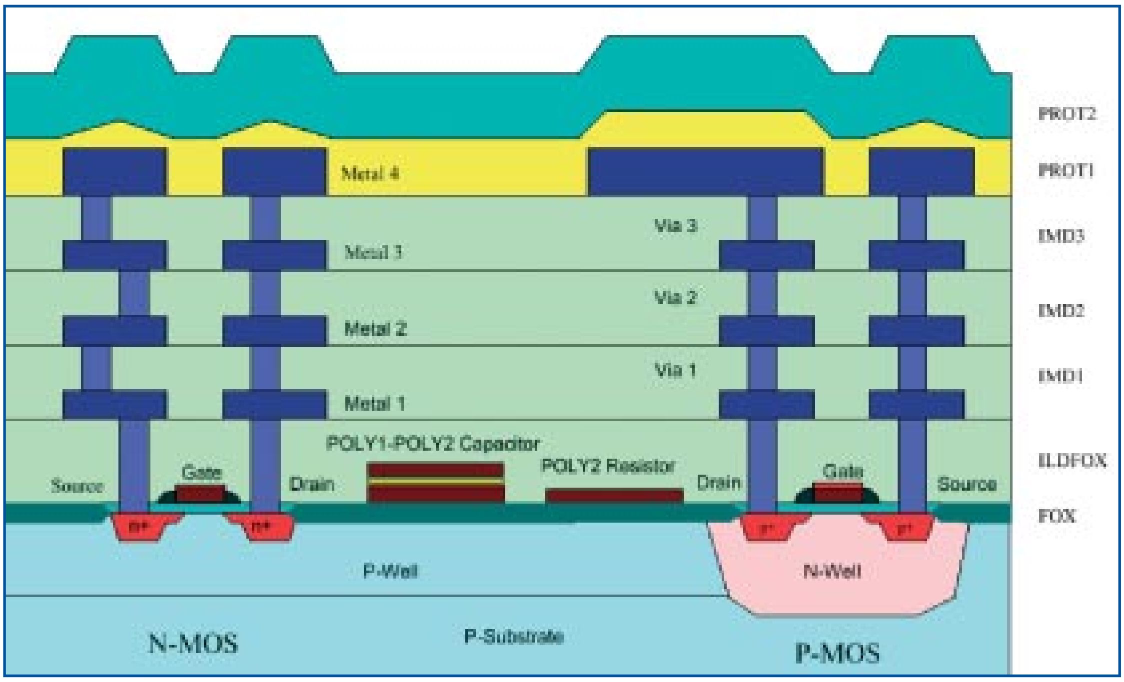
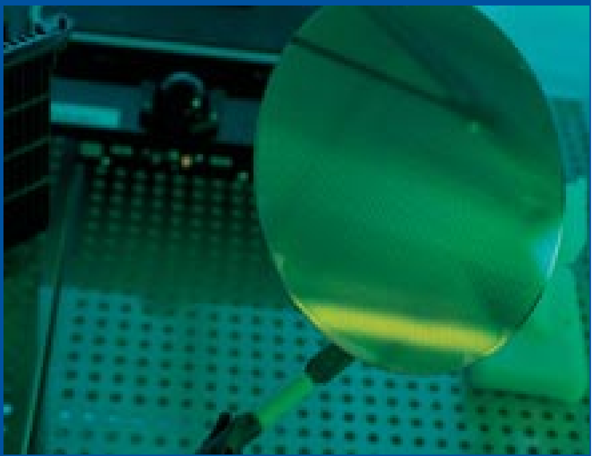


Fig. 1: Schematic cross-section of a modern silicon IC; vias (tungsten plugs); gates (tungsten silicide); four layers of metal interconnect (Al). *By courtesy of austriamicrosystems AG, AMS.*

Fig. 2:

(a) Wafer in production; still missing interconnects and wiring plains



(b) Finished Wafer already cut; chips are removed automatically.

By courtesy of austriamicrosystems AG, AMS.

Several main operations are the basis of chip making: oxidation, ion implantation and diffusion, deposition of thin films (by chemical vapor deposition [CVD] or physical vapor deposition [PVD]), electro plating, patterning (photolithography) and etching (can be also combined with mechanical polishing). Between these steps sometimes a Rapid Thermal Processing is applied for changing the characteristics of the deposited film. Another in-between step can be Chemical Mechanical Polishing to produce a planar surface of the deposited layer. Processing of a chip may vary from a few days to up to three months requiring a careful testing at each step of the process.

The basis of a chip is a silicon plate or substrate, also named wafer (purity 99.99999999 %). Above processes and sometimes some more are repeated many times on the base resulting in the build-up of microscopically thin layers of different materials. After completion a single wafer will contain hundreds of individual chips ***(Fig 2)*** that can be tested on the wafer level for their properties, cut from the wafer, packaged and assembled ***(Fig. 3)***. Prior to shipment a final test is usually performed on the assembled parts.

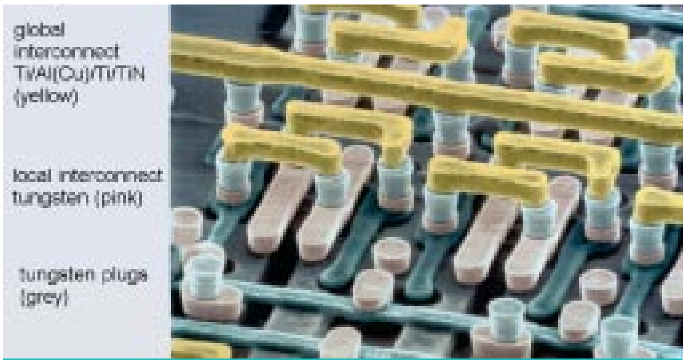
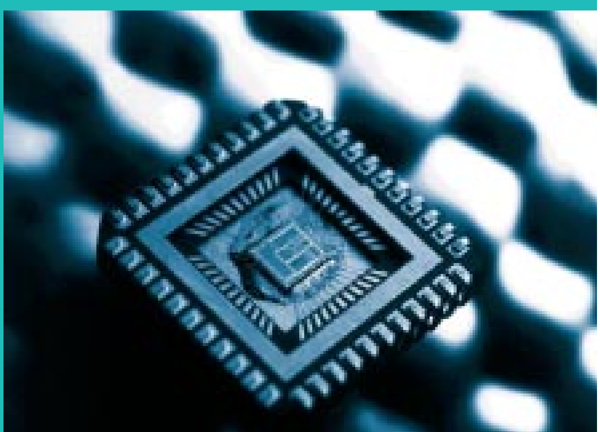


Fig. 4: "Tiny Highways" provide the interconnections among individual transistors and other devices of a chip. Low-angle scanning electron micrograph of a portion of a partially completed SRAM array (static random access memory) containing six-device memory cells. The insulating oxide films have been removed, revealing the lower levels of the interconnection structure of the array.

Local interconnections made of tungsten provide cross-coupling for the n+ and p+ diffusion contacts. Tungsten contact studs (plugs) constitute the upper portions of the contact paths to the global interconnections.

By courtesy of IBM, USA; http://www-3.ibm.com/chips/technology/

Fig.3: Assembled chip; chip is in the middle; contacts by gold and/or aluminium wires to outside.



By courtesy of austriamicrosystems AG, AMS.

Tungsten is applied as tungsten metal, tungsten silicide, tungsten nitride and tungsten titanium alloy thin films or plugs ***(see Fig. 4)***. The deposition is performed either by CVD or PVD. The dimensions of these components vary depending on chip application between nm and µm.

As size measure for a special technology acts the Minimum Feature Size which corresponds to the minimum drawn channel length in MOS (metal–oxide-semiconductor) transistors. According to Moore’s Law, in the course of development it decreased every third year by the factor 0.7 (from 250 nm in 1997 to 130 nm in 2003), whereas the chip size increased by 16 % yearly. By that the performance of a chip in average is doubled every $1^1/_2$ years. It is assumed that the minimum feature size will further decrease to 50 nm until 2012. The ultimate limit appears today to be 25 nm. The smaller the size gets the more sensitive the process becomes in regard to materials and layer properties.An example for an electronic equipment which contains a chip with feature size < 150 nm and which is known to everybody is the today's mobile phone. Another well known example is the 2.2 GHz Pentium®, 4 processor that consists of 55 million transistors with structure sizes as small as 60 nm and six layers of Cu interconnects with an overall lengths of more than three kilometres of internal "wiring".

TUNGSTEN SOURCES

Tungsten Hexafluoride: WF_6

The main source for tungsten applications in microelectronics is tungsten hexafluoride. It serves in chemical vapor deposition (CVD) of tungsten or tungsten silicide as thin films or plugs. Its most convenient production procedure is the direct fluorination of tungsten at 350 –400 °C in a flowing system according to the equation

$$W + 3F_2 \rightarrow WF_6$$

It is a white solid below 2.0°C, a pale yellow liquid up to 17.2°C and a colorless gas above. It is one of the heaviest gases known (149 times heavier than hydrogen).

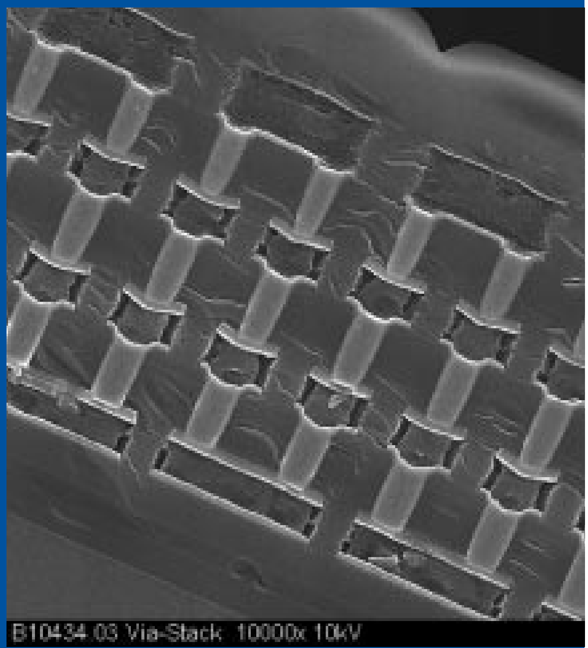
It is very reactive, attacks most metals and also glass and decomposes in the presence of water vapor.

Crucial for its application in microelectronics production is the purity which ranges depending on application between 99.98% (electronic), 99.998% (VLSI = very large scale integration) and 99.9998% (megaclass). The annual consumption worldwide can be estimated to be around 200 t and is steadily growing due to the constant increase in electronics production.

Sputter Targets

Another tungsten source are sputter targets of tungsten metal, tungsten silicide and tungsten titanium alloy for physical vapor deposition (PVD). Also in this application highest purity is crucial. 6N tungsten powder, that means a purity of 99.9999%, is commercially available today for target production. In particular the uranium and thorium contents must be very low (<0.3 ng/g). Due to their α-particle emission they cause "soft errors" in memory circuits. Not only the purity is important, but also density, surface cleanliness and microstructure. These properties are responsible for particle generation during sputtering, which should be extremely low.

Fig. 5: SEM micrograph of a four level metal process using tungsten plugs; tungsten plugs are the vertical conductive layers used to connect one horizontal layer of conductors with another horizontal layer of conductors on a chip.



By courtesy of austriamicrosystems AG, AMS.

DEPOSITION OF TUNGSTEN

All advanced chips rely on tungsten contacts (vias, plugs) to connect the transistor and the interconnecting layers (see scheme in ***Fig. 1*** and SEM micrographs in ***Fig.4, 5***). Sometimes also interconnect layers itself consist of tungsten. The properties which make tungsten the preferred material for that purpose are: low resistance, low stress, excellent conformal step coverage, nearly equal thermal expansion coefficient as silicon, good electromigration resistance and low resistance contacts to silicon. The void for the plug prior to tungsten deposition has to be coated by a thin layer of Ti/TiN as diffusion barrier. As well CVD and PVD are used to deposit tungsten, but the first method is preferred, because of better process control especially for smaller dimensions.

In PVD argon ions produced from a gun are shot under vacuum on the target liberating target atoms which deposit on the substrate.

The principle of CVD is that the two gaseous reactants are mixed very close above the substrate surface, where the solid tungsten is deposited at elevated temperature.

The chemical reaction for the tungsten CVD process is shown in the equation

$$WF_6 + 3H_2 \rightarrow W + 6HF$$

HF formed during the reaction locally may form defects like wormholes and encroachment, giving the possibility to foreign atoms to migrate to the semiconductor. Therefore, in the beginning of the tungsten deposition silane (SiH_4) is used as reducing agent to produce a thin first tungsten nucleation layer. As long as the molar ratio of tungsten hexafluoride and silane is kept below 1, α-tungsten is deposited and no silicon. The reaction with silane is much faster as with hydrogen and results in a tungsten film with good adhesion and none of the above defects. The further filling of the void is done by hydrogen reduction. The deposition is performed in special equipment under low pressure at temperatures ranging between 250 and 500 °C.

Fig. 6: SEM micrograph of a transistor using a tungsten silicide gate (cross sectional view).

By courtesy of austriamicrosystems AG, AMS.

In order to fill the void for the plug completely an overfill and a subsequent etch back will be necessary to end up in a planar surface.

In case of 90 nm technology and also for lower gate dimensions a special process named ALD (Atomic Layer Deposition) is applied to deposit the first film. In principle it is also a CVD process but using more sophisticated equipment and running under very low pressure and flow rate of the reactant gases in very short process steps (approx. 100 msec) at 300-350 °C. The growth rate per cycle is 2.5-3.0 Å. The process uses diborane instead of silane as reducing agent and provides a 100 % step coverage also at aspect ratios of 20:1 and more.

DEPOSITION OF WSi_x (x = 2.55-3.00)

Tungsten silicide is applied in gate electrodes (see scheme in ***Fig.1*** and SEM micrograph in ***Fig. 6***) down to a feature size of 0.35µm. For smaller dimensions silicides of cobalt or titanium are in use. Tungsten silicide lowers the gate resistance and thus the gate delay time. And, therefore, it is responsible for the basic function (speed) of an integrated circuit .

The following properties are responsible for the use of tungsten silicide in above applications:

- electric resistivity 30 µΩ·cm

- extreme short gate delay time ($10^{-9} – 10^{-10}$ sec).

The requirements for the film are: uniform film composition across the interface and the bulk of the film, low stress as deposited and annealed and low F and Cl impurities. Moreover, a high step coverage, no cracks after anneal, excellent adhesion and no delamination are of importance.

In principle there are two methods in use to deposit WSi_x. One is to reduce tungsten hexafluoride with silane at 400°C. This is the same process as described for the deposition of tungsten metal, but the molar ratio of the reactants is shifted more to the side of silane. The reaction is symbolized in the equation

$$a\ WF_6 + b\ SiH_4 \rightarrow c\ WSi_x + d\ SiF_4 + f\ H_2$$

The second method uses dichlorsilane as reducing agent at 550°C and the reaction is given in the equation

$$a'\ WF_6 + b'\ SiH_2Cl_2 \rightarrow c'\ WSi_x + d'\ SiF_4 + f'\ SiCl_4 + g'\ HCl + h'\ H_2$$

The silane process is stable due to the high reactivity of the reacting gases and insensitive to wafer surface conditions. The fluorine concentrations in the deposited layer are higher as in the dichlorosilane process. The layer has a low step coverage and an instability during annealing, because the as deposited layer is amorphous and recrystallizes on heating.

The dichlorosilane process, due to a decreased reactivity of the two compounds, results in highest quality tungsten silicide layer with good step coverage, less impurities and a polycrystalline layer, resulting in much less stress after anneal. But the process is less stable, less robust and depends on the surface properties, on temperature and substrate type.

For even lower resistivity gates and to reduce the RC delay tungsten/tungsten nitride is in use.

TUNGSTEN DEMAND

The tungsten demand for integrated circuits due to the thin films and the miniaturization is in general very low, but the effects of this small quantity are enormous if we consider all the possibilities which are offered today by microelectronic equipment and their world wide dense distribution.

Most of the tungsten input in chip technology gets lost by deposition on masks and equipment parts and also by subsequent etching or polishing.

After all we should ask - *how much tungsten is contained in a chip?* It depends mainly on its dimension and its feature size. A rough estimation reveals that a plug in a common device corresponds to $2 \cdot 10^{-14}$ g W and a gate is even less. If we assume to be 10^{6} plugs and gates in a chip, it would correspond to approx. 10^{-8} g W. Compared to other tungsten consumers it is only a homeopathic dose or a little bit more than nothing. But it is an essential part of a chip and a chip is a very important tool in today's human life.

ACKNOWLEDGEMENT:
For valuable information, literature and photographs the authors feel kindly indebted to austriamicrosystems AG.; AMS, A-8141 Unterpremstätten, Austria, especially to Dipl. Ing. Ewald Stueckler and to IBM for providing the copyright for Figure 4.

Further reading: all major chip producers provide web information on both chip manufacture and development.

The Economics of Tungsten, 8th Edition, 2003

Written and published by Roskill Information Services, this is not only an authoritative guide to the tungsten industry and the market but also a valuable reference source. The book provides

- A market analysis of consumption, regional and worldwide, and of demand and the end-use markets;
- A production report on reserves, resources, output and capacity in each country;
- A company profile giving up-to-date information on the activities of the major producing and processing companies;
- A comprehensive statistical source with 103 tables.

Copies may be obtained, at a price of £1,400 / $ 2,800 / €2,450, from

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10th International Tungsten Symposium

This event will be held during the week beginning 19 September 2005 in Changsha, China and will be hosted by Zhuzhou Cemented Carbide Group Corp., Ltd and Minmetals.

Please note the amended date.

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